Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.129”**

**PAD FUNCTIONS:**

1. **V IN (2 bond pads)**
2. **V OUT (2 bond pads)**
3. **V OUT SENSE**
4. **ADJUST**

**Table

Description automatically generated with low confidence**

**Top Material: Al**

**Backside Material: Ti/Ni/Au**

**Bond Pad Size: 0.00905 X 0.00905” min.**

**Backside Potential:**

**Mask Ref: VIN**

**APPROVED BY: KW DIE SIZE .075” X .075 X .011” DATE: 10/12/22**

**MFG: SILICON SUPPLIES THICKNESS P/N: MC7905**

**DG 10.1.2**

#### Rev B, 7/19/02